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09/526,394	03/16/2000	Wayne J. Howell	BU9-99-175	1550

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/526,394	Applicant(s) HOWELL ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,6,9,10,13 and 15-31* is/are pending in the application.

4a) Of the above claim(s) *15-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,6,9,10,13 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Clams 9 and 10 are objected to under 37 CFR 1.75(c), as being of improper dependent form, as being dependent on previously cancelled independent claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

A. Claim 2 recites the limitation "said same material" in line 1.

B. Claim 13 recites the limitation "said metal plug" in line 14.

There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 6, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732) in view of Mori et al. (US Pat. 6335570).

Regarding claim 6, Kumar et al. disclose a metallurgical/conductive structure in an integrated circuit (IC) chip having underlying circuitry/internal components within an exterior covering comprising:

- a first layer/line/metal pad/internal component (14b in Fig. 10) on the chip/substrate
- a passivation/insulating layer (16b in Fig. 10)
- a via/hole (Fig. 10) through the passivation layer extending to the first layer/metal pad/line
- a barrier layer/first barrier layer lining the via (18b in Fig. 10), and
- a metal plug/bump/second layer (40b in Fig. 10; 40 in Fig. 9) in the via above the barrier layer wherein the metal plug/bump, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure,
- the metal plug/bump being of predetermined thickness and being made of material such as copper (Col. 5, line 44)
- solder bump/connector/conductive structure (44 in Fig. 10; Col. 6, line 10) comprising a tin/lead alloy, the solder bump being in direct contact with the

- conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface

(Fig. 10; Col. 5, line 23- Col. 6, line 15; Fig. 5-10; Col. 3-12).

Kumar et al. further disclose the conductive structure having the solder bump/connector where the barrier layer comprises an adhesion/barrier material such as Ti, TiN, TaN, nickel, etc. with a copper plug of predetermined/sufficient thickness is used to reduce/prevent the diffusion of elements/species/metals such as tin, present within the solder bump/conductive structure into the metal line to provide low contact resistance and improved adhesion/reliability (Col. 3, line 36-68; Col. 3-6).

Kumar et al. fail to teach using a second barrier layer above the first metal plug and a second metal above the second barrier layer such that the second metal plug and the first and second barrier layers form a planar exterior surface.

Mori et al. teach using a multilevel copper plug structure to provide an improved/more effective protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization where the multilevel copper plug structure comprises a second barrier layer (42 in Fig. 18) above the first metal plug (5 in Fig. 18) and a second metal (10 in Fig. 18) above the second barrier layer (Fig. 18-22; Col. 9, line 13- Col. 10, line 5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the first metal plug and a second metal above the second barrier layer such that the second metal plug and the first and second barrier layers form a planar exterior surface as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Kumar et al's structure.

Regarding claim 3, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, wherein Kumar et al. further teach the first barrier layer comprising one or more layers of titanium (Ti), titanium nitride (TiN), tantalum (Ta) and tantalum nitride (TaN) to provide the diffusion barrier between the solder bump metals/species such as tin and the metal pad/line (Col. 3, line 30- Col. 4, line 11), but fail to teach the second barrier layer comprising one or more layers of Ti, TiN, Ta and TaN .

Mori et al. further teach using a plurality of barrier layers including the first and second barrier layers (4 and 42 respectively in Fig. 18; Col. 6, line 17, Col. 9, line 57) comprising TaN .

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first and second barrier layers comprising one or more layers of Ti, TiN, Ta and TaN as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Kumar et al's structure.

Regarding claim 29, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, wherein Kumar et al. further teach solder bump (44 in Fig. 10; Col. 6, line 10) comprising the tin/lead alloy.

Regarding claim 30, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, except the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the metal line.

Mori et al. teach using a multilevel copper plug structure to provide an improved/more effective protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization where the multilevel copper plug structure comprises a second barrier layer (42 in Fig. 18) above the first metal plug (5 in Fig. 18) and a second metal (10 in Fig. 18) above the second barrier layer (Fig. 18-22; Col. 9, line 13- Col. 10, line 5).

It is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to one of ordinary skill in the art to recognize that such double/multi-level layers of copper metal/plug having predetermined/sufficient thickness would form a desired quantity/sufficient intermetallics with elements of the solder such as tin so that the desired level of protection against penetration/diffusion of the elements through the first and second barrier layers is achieved as taught by Mori et al. in Kumar et al's structure.

5. Claims 13, 22-28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Pat. 5290732) in view of Mori et al. (US Pat. 6335570) and Zhao et al. (US Pat. 5674787).

Regarding claim 13, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, except:

a) the first plug, the second plug and the internal components comprising the same material, and

b) the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the internal components.

a) Zhao et al. teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

b) Mori et al. teach using a multilevel copper plug structure to provide an improved/more effective protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization where the multilevel copper plug structure comprises a second barrier layer (42 in Fig. 18) above the first metal plug (5 in Fig. 18) and a second metal (10 in Fig. 18) above the second barrier layer (Fig. 18-22; Col. 9, line 13- Col. 10, line 5).

Furthermore, it is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the second plug and the internal components comprising the same material as taught by Zhao et al. and the second metal plug forming sufficient intermetallics with elements diffusing from the solder bump so as to prevent the elements from penetrating through the first and second barrier layers into the internal components as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Kumar et al's structure.

Regarding claim 22, Kumar et al., Mori et al. and Zhao et al. teach substantially the entire claimed structure as applied to claims 13 and 6 above, wherein Kumar et al. further teach the connector (44 in Fig. 10; Col. 6, line 10) being comprised of the tin/lead alloy.

Regarding claim 23, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, except:
a) the first layer and the second layer being copper, and
b) the third layer of copper being formed on the second barrier layer, the second layer of copper having a thickness sufficient to form intermetallics with species diffusing from the conductive structure and to adhere to the conductive structure, so as to prevent the species from penetrating through the first barrier layer into the first layer of copper.

a) Zhao et al. teach using a conductive structure where a metal plug/second layer (23 in Fig. 6) and a metal line/first layer comprises a conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

b) Mori et al. teach using a multilevel copper plug structure having predetermined/sufficiently thick layers of copper to provide an improved/more effective protection against diffusion of copper compounds/intermetallics into underlying insulating layers and metalization where the multilevel copper plug structure comprises a second barrier layer (42 in Fig. 18) above the first metal plug/second layer (5 in Fig. 18) and a second metal/third layer (10 in Fig. 18) above the second barrier layer (Fig. 18-22; Col. 9, line 13- Col. 10, line 5).

Furthermore, it is well known in chip packaging and interconnection technology art that copper readily reacts and forms intermetallics with elements such as tin from the solder (see admitted prior art- specification page 3, line 12; pages 3 and 4).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the first layer and the second layer being copper as taught by Zhao et al. and the third layer of copper being formed on the second barrier layer, the second layer of copper having a thickness sufficient to form intermetallics with species diffusing from the conductive structure and to adhere to the conductive structure, so as to prevent the species from penetrating through the first barrier layer into the first layer of copper as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Zhao et al. and Kumar et al's structure.

Regarding claims 24-26, Kumar et al., Mori et al. and Zhao et al. teach substantially the entire claimed structure as applied to claim 23 above, wherein Kumar et al. further teach the conductive structure comprising the solder ball made of the tin/lead alloy having elements/species such as tin (44 in Fig. 10; Col. 6, line 10).

Regarding claim 27, Kumar et al., Zhao et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 23 above, wherein Kumar et al. further teach the first barrier layer comprising one or more layers of titanium (Ti), titanium nitride (TiN), tantalum (Ta) and tantalum nitride (TaN) to provide the diffusion barrier between the solder bump metals/species such as tin and the metal pad/line (Col. 3, line 30- Col. 4, line 11), but fail to teach the second barrier layer comprising one or more layers of Ti, TiN, Ta and TaN .

Mori et al. further teach using a plurality of barrier layers including the first and second barrier layers (4 and 42 respectively in Fig. 18; Col. 6, line 17, Col. 9, line 57) comprising TaN .

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first and second barrier layers comprising one or more layers of Ti, TiN, Ta and TaN as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Zhao et al. and Kumar et al's structure.

Regarding claims 28 and 31, Kumar et al., Zhao et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 23 above, wherein Kumar et al. further teach the copper metal plug/second layer having an upper surface being substantially coplanar with the surrounding insulative structures (Fig. 10), but fail to teach a third layer of copper being substantially coplanar or being planarized with the surrounding insulative structures.

Mori et al. further teach the multilevel copper plug structure having an upper surface of copper (124 in Fig. 38) being subjected to chemical-mechanical polishing/planarizing (CMP) to provide a substantially coplanar surface with the surrounding insulative structures (Col. 2, lines 15-25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the third layer of copper being substantially coplanar with the surrounding insulative structures as taught by Mori et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Zhao et al. and Kumar et al's structure.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (US Pat. 5290732) and Mori et al. (US Pat. 6335570) as applied to claim 6 above, and further in view of Zhao et al. (US Pat. 5674787).

Regarding claim 2, Kumar et al. and Mori et al. teach substantially the entire claimed structure as applied to claim 6 above, except the metal line and the first metal plug comprising copper.

Zhao et al. teach using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (23/11 in Fig. 6; Col. 5, line 22; Col. 7, line 25).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal line and the first metal plug comprising copper as taught by Zhao et al. so that the desired electrical resistance and the protection/barrier against the diffusion of intermetallics and the dielectric layer integrity can be improved in Mori et al. and Kumar et al's structures.

Response to Arguments

7. Applicant's arguments with respect to claims 2, 3, 6, 9, 10, 13 and 22-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

NP

Nitin Parekh
07-02-03

Tom Thomas

TOM THOMAS
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